In the Claims:

All of the currently pending claims are listed below including any amendments proposed herein. Please amend the claims as follows:

Please cancel claims 1-4 without prejudice.

1-4. (Canceled)

5. (Currently amended) A basic input/output system (BIOS) for use in a computer system having a plurality of processors and a system memory, the BIOS being embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous testing of different portions of the system memory by selected ones of the plurality of processors, wherein one of the plurality of processors comprises a boot strap processor, and wherein the plurality of processors are configured in a plurality of multi-processor clusters, each of the clusters corresponding to at least one of the different portions of the system memory, ~~The BIOS of claim 3~~ wherein the computer program instructions are operable to cause the boot strap processor to assign only one of the processors in each cluster to the corresponding portion of the system memory.

Please cancel claims 6-9 without prejudice.

6-9. (Canceled)

10. (Currently amended) A basic input/output system (BIOS) for use in a computer system having a plurality of processors and a system memory, the BIOS being embodied in a

computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous testing of different portions of the system memory by selected ones of the plurality of processors, wherein one of the plurality of processors comprises a boot strap processor, the computer program instructions being further operable to cause the boot strap processor to assign each of the different portions of the system memory to one of the selected processors, and to instruct the selected processors to begin testing of the system memory, the computer program instructions further being operable to cause each of the selected processors to initialize and validate its assigned portion of the system memory, to report memory testing progress to the boot strap processor, and ~~The BIOS of claim 8 wherein the computer program instructions are operable to cause each of the selected processors~~ to update the memory testing progress periodically.

11. (Original) The BIOS of claim 10 wherein the computer program instructions are operable to cause each of the selected processors to update the memory testing progress after testing a memory segment in its assigned portion of the system memory.

Please cancel claim 12 without prejudice.

12. (Canceled)

13. (Currently amended) A basic input/output system (BIOS) for use in a computer system having a plurality of processors and a system memory, the BIOS being embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous testing of different portions of the system memory by selected ones of the plurality of processors, wherein one of the plurality of processors comprises a boot strap

processor, the computer program instructions being further operable to cause the boot strap processor to assign each of the different portions of the system memory to one of the selected processors, to monitor progress in testing of the system memory by the selected processors, and ~~The BIOS of claim 12 wherein the computer program instructions are operable to cause the boot strap processor~~ to periodically update status information corresponding to the progress.

14. (Original) The BIOS of claim 13 wherein the computer program instructions are operable to cause the boot strap processor to update the status information after testing a memory segment in its assigned portion of the system memory.

Please cancel claims 15 and 16 without prejudice.

15-16. (Canceled)

17. (Currently amended) A basic input/output system (BIOS) for use in a computer system having a plurality of processors and a system memory, the BIOS being embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous testing of different portions of the system memory by selected ones of the plurality of processors, wherein one of the plurality of processors comprises a boot strap processor, the computer program instructions being further operable to cause the boot strap processor to assign each of the different portions of the system memory to one of the selected processors, to generate memory testing results upon completion of the testing of the system memory by the selected processors, and to disable any memory modules corresponding to corrupted memory ranges indicated in the memory testing results, ~~The BIOS of claim 16~~ wherein

the computer program instructions are further operable to cause the computer system to reboot after disabling the memory modules.

18. (Currently amended) A basic input/output system (BIOS) for use in a computer system having a plurality of processors and a system memory, the BIOS being embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous testing of different portions of the system memory by selected ones of the plurality of processors, wherein one of the plurality of processors comprises a boot strap processor, the computer program instructions being further operable to cause the boot strap processor to assign each of the different portions of the system memory to one of the selected processors, and ~~The BIOS of claim 2 wherein the computer program instructions are operable to cause the boot strap processor~~ to allocate separate stack memory in a shared memory for each of the selected processors.

19. (Currently amended) A basic input/output system (BIOS) for use in a computer system having a plurality of processors and a system memory, the BIOS being embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous testing of different portions of the system memory by selected ones of the plurality of processors, wherein one of the plurality of processors comprises a boot strap processor, the computer program instructions being further operable to cause the boot strap processor to assign each of the different portions of the system memory to one of the selected processors, and ~~The BIOS of claim 2 wherein the computer program instructions are operable to cause the boot strap processor~~ to disable interrupt generation by the selected processors.

20. (Currently amended) A basic input/output system (BIOS) for use in a computer system having a plurality of processors and a system memory, the BIOS being embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous testing of different portions of the system memory by selected ones of the plurality of processors, wherein one of the plurality of processors comprises a boot strap processor, the computer program instructions being further operable to cause the boot strap processor to assign each of the different portions of the system memory to one of the selected processors, and ~~The BIOS of claim 2~~ wherein the computer program instructions are further operable to associate a lock prefix with instructions targeting a shared memory associated with the boot strap processor thereby ensuring that two of the processors do not access the shared memory at the same time.

Please cancel claims 21-33without prejudice.

21-33. (Canceled)